Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (currently amended) An embedded computing system, comprising:

a plurality of processors;

a bus coupling to a plurality of peripheral units;

a multiplexor for coupling each of the plurality of processors to the bus in response to an owner signal; and

a set of peripheral-share registers wherein each member of the set resides at and is associated with a particular one of the plurality of peripheral units and includes an entry ~~associated with each of the plurality of peripheral units~~ holding a state value indicating which of the plurality of processors currently owns the ~~associated~~ peripheral unit, wherein the owner signal is based on one of the state values such that only the one of the processors indicated as currently owning the peripheral is coupled by the multiplexor to the peripheral.

2. (original) The system of claim 1, wherein the multiplexor is bi-directional and comprises:

an address multiplexor coupled to address outputs of each of the plurality of processors wherein the address multiplexor selectively couples one of the processor address outputs to a MUX address output based on the state of the owner signal;

a data multiplexor coupled to data outputs of each of the plurality of processors, wherein the data multiplexor selectively couples one of the processor data outputs to a MUX data output based on the state of the owner signal; and

a shared register having an address port coupled to the MUX address output, a data port coupled to the MUX data output, and a bus port coupled to communicate with the bus.

3. (original) The controller of claim 1, wherein one of the processors is dedicated to executing operating system code and another one of the processors is executing application code.

4. (original) The controller of claim 1 wherein the set of peripheral share registers includes a plurality of request registers such that each request register corresponds to one of the plurality of processors, wherein each request register has an entry associated with each of the peripheral units, and wherein each entry holds a value indicating whether the corresponding processor is requesting ownership of the associated peripheral unit.

5. (original) The controller of claim 1 wherein the set of peripheral share registers includes a plurality of release registers such that each release register corresponds to one of the plurality of processors, wherein each release register has an entry associated with each of the peripheral units, and wherein each entry holds a value indicating whether the corresponding processor is releasing ownership of the associated peripheral unit.

6. (original) The controller of claim 1 wherein the set of peripheral share registers includes a priority register having an entry associated with each of the peripheral units, wherein each entry holds a value indicating which of the plurality of processors wins ownership of the associated peripheral unit when a conflict occurs between two or more of the processors requesting ownership of the associated peripheral unit.

7. (original) The controller of claim 1, wherein the system further comprises the peripheral units and wherein the processors and the peripheral units comprise a single integrated circuit.

8. (original) The controller of claim 1 wherein the state value is dynamically configurable during operation by at least one of the plurality of processors.

Claims 9-12 (canceled)

13. (currently amended) A multiprocessor controller, comprising:

first and second processor cores;

a plurality of peripherals;

a bus coupling the processor cores to the peripherals; and

means for arbitrating between the processor cores for communication access to requested ones of the peripherals, whereby each of the peripherals is only used by one of the core processors at a particular time, wherein the arbitrating means comprises logic for determining which of the processor cores is an owner of a requested one of the peripherals, wherein the arbitrating means further comprises a multiplexor for selectably coupling the processor cores to the bus in response to an owner signal, the multiplexor comprising:

an address multiplexor coupled to address outputs of the processor cores wherein the address multiplexor selectively couples one of the processor address outputs to a MUX address output based on a state of the owner signal; and

a data multiplexor coupled to data outputs of the processor cores, wherein the data multiplexor selectively couples one of the processor data outputs to a MUX data output based on the state of the owner signal; and

a set of peripheral-share registers wherein ~~a first~~ each member of the set resides at and is associated with one of the plurality of peripherals and includes an entry ~~associated with each of the plurality of peripheral units~~ that holds a state value indicating which of the processor cores currently owns the associated peripheral.

14. (original) The controller of claim 13, wherein the bus comprises an address bus and a data bus for each of the processor cores.

15. (original) The controller of claim 14, wherein the arbitrating means further comprises a multiplexor for selecting the address and data busses corresponding to one of the core processors to the bus in response to an owner signal corresponding to the ownership determination.

16. (original) The controller of claim 13, wherein the arbitrating means further comprises a control register for each of the peripherals storing an ownership state indicating which of the core processors controls ownership.

17. (canceled)

18. (original) The controller of claim 13, wherein the processor cores comprise embedded processor cores integrated on a single integrated circuit chip.

19. (original) The controller of claim 18, further comprising:

a peripheral control register associated with each of the peripheral units, wherein the peripheral control register is shared amongst the plurality of processors and is integrated on the single integrated circuit chip.

Claims 20-24 (canceled)

25. (currently amended) A multiprocessor computing system, comprising:

a pair of processors;

a plurality of peripheral units;

a bus coupling to each of the peripheral units; [[and]]

a multiplexor selectively coupling each of the processors to the bus, wherein the processors, the peripheral units, and the multiplexor comprise a single integrated circuit[[.]] ;

in the integrated circuit, a peripheral register associated with each of the peripheral units including an entry associated with each of the processors holding a state value indicating which one of the processors owns the associated peripheral unit, wherein the multiplexor performs the coupling based on the state values in the peripheral registers.

26. (canceled)

27. (currently amended) The system of claim [[26]] 25, wherein the state value is dynamically configurable during operation by at least one of the processors.

28. (original) The system of claim 25, wherein the multiplexor is bi-directional and comprises:

an address multiplexor coupled to address outputs of each of the processors wherein the address multiplexor selectively couples one of the processor address outputs to a MUX address output based on the state of the owner signal;

a data multiplexor coupled to data outputs of each of the processors, wherein the data multiplexor selectively couples one of the processor data outputs to a MUX data output based on the state of the owner signal; and

a shared register having an address port coupled to the MUX address output, a data port coupled to the MUX data output, and a bus port coupled to communicate with the bus.

29. (previously presented) The system of claim 28, wherein the set of peripheral share registers includes a plurality of request registers such that each request register corresponds to one of the processors, wherein each request register has an entry associated with each of the peripheral units, and wherein each entry holds a value indicating whether the corresponding processor is requesting ownership of the associated peripheral unit.

30. (original) The system of claim 25, wherein one of the processors is dedicated to executing operating system code and another one of the processors is executing application code.